(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 544 069 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 92115194.0

(22) Date of filing: 04.09.92

(51) Int. Cl.5: G02F 1/136, H01L 29/784, H01L 21/336

(30) Priority: 26.11.91 JP 335553/91
27.11.91 JP 335875/91
13.12.91 JP 351328/91

(43) Date of publication of application:
02.06.93 Bulletin 93/22

(84) Designated Contracting States:
DE FR GB IT NL

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(54) Thin-film transistor panel and method of manufacturing the same.

(57) A thin-film transistor panel comprises an insulative substrate (11), a plurality of thin-film transistor elements (10) arranged at predetermined intervals on said substrate, and wirings (DL, GL) electrically connecting the thin-film transistor elements characterized in that the thin-film transistor element comprises a gate electrode (12G), a gate-insulating film (13), an i-type semiconductor layer to face the gate electrode through the gate insulating film therebetween, an n-type semiconductor layer, a source and drain electrodes (16S, 16D) electrically connected the portions of the i-type semiconductor layer through the n-type semiconductor layer, and an anodically oxidized film (15a) located between the source and drain electrodes to electrically isolate, said source and drain electrodes.

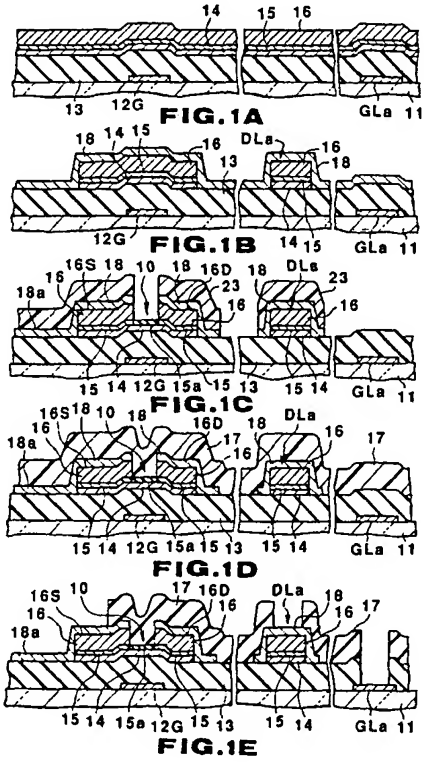

FIG.1A
FIG.1B
FIG.1C
FIG.1D
FIG.1E

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The present invention relates to a thin-film transistor panel for use in an active matrix liquid-crystal display.

Generally, a thin-film transistor panel (herein after referred to as "TFT panel") designed for use in an active matrix liquid-crystal display, has a specific structure which will be described with reference to Figs. 10 to 13.

Fig. 10 is a plan view showing a part of the TFT panel, and Figs. 11, 12 and 13 are enlarged, cross-sectional views of the TFT panel, taken along lines XI-XI, XII-XII and XIII-XIII in Fig. 10, respectively.

The conventional TFT panel comprises a transparent substrate 1 made of glass or the like, a number of pixel electrodes 8a formed on the substrate 1, a number of thin-film transistors (TFTs) 0 functioning as active elements, a gate line GL connected to the gate electrodes 2G of the thin-film transistors 0, and a drain line (i.e., data line) DL connected to the drain electrodes 6D of the thin-film transistors 0.

The thin-film transistors 0 have a structure generally known as "inverse stagger structure." As is shown in Figs. 10 and 11, each thin-film transistor comprises a gate electrode 2G formed on the substrate 1, a gate-insulating film 3 covering the gate electrode 2G, an i-type semiconductor layer 4 formed on the gate-insulating film 3 and opposing the gate electrode 2G, an n-type semiconductor layer 5 formed on the i-type semiconductor layer 4, a source electrode 6S formed on one end portion of the n-type semiconductor layer 5, a drain electrode 6D formed on the other end portion of the n-type semiconductor layer 5. The channel region (i.e., the portion extending between the electrodes 6S and 6D) of the i-type semiconductor layer 4 has been removed, forming two i-type semiconductor layers.

The gate electrode 2G is integral with the gate line GL formed on the substrate 1. The gate line GL and the gate electrode 2G are made of metal such as Al, an Al alloy, Cr, or Ta. The gate-insulating film 3 is made of SiN (silicon nitride) or the like. The i-type semiconductor layer 4 is made of a-Si (amorphous silicon), and the n-type semiconductor layer 5 is made of a-Si doped with an n-type impurity.

A blocking layer made of SiN or the like is formed on the channel region of the i-type semiconductor layer 4. The blocking insulation layer 7 is provided to prevent the channel region of the i-type semiconductor layer 4 from being when the corresponding region of the n-type semiconductor layer 5 formed on the layer 4 is etched.

The gate-insulating film 3 of each thin-film transistor 0 is formed on the substrate 1, covering the gate line GL. The pixel electrode 8a and the drain lien DL are formed on the gate-insulating (transparent) film 3.

The drain line DL is integral with the drain electrode 6D of each thing-film transistor 0. The drain line DL, the drain electrode 6D, and the source electrode 6S are made of metal such as Al, an Al alloy, Cr, or Ta.

The pixel electrode 8a is formed of a transparent conductive film of ITO or the like. This electrode 8a has one terminal portion located on the source electrode 65 and, hence, is electrically connected to the source electrode 6S.

Thin-film transistor 0 and the drain line DL on the gate-insulating film 3 are covered with a protective insulation film 9 which is made of SiN or the like. The film 9 is formed on the entire surface of the substrate 1, except for the pixel electrode 8a. The terminal portion DLa of the drain line DL is exposed by removing that portion of the film 9 which is located above the portion DLa, as is shown in Figs. 10 and 12. The terminal portion GLa of the gate line GL is exposed by removing that portion of the gate-insulating film 3 which is located on the terminal protion GLa and also that portion of the protective insulation film 9 which us located above the terminal portion GLa, as is shown in Figs. 10 and 13.

The conventional TFT panel is manufactred by the following method.

[Step 1]

First, a gate-forming metal film is formed on the substrate 1. This metal film is patterned by photolithography, thereby forming the gate lines GL and the gate electrode 2G.

[Step 2]

The gate-insulating film 3 is formed on the substrate 1, covering the gate lines GL and the gate electrode 2G. Further, the i-type semiconductor layer 4 is formed on the gate-insulating film 3, and the blocking layer 7 is formed on the i-type semiconductor layer 4.

[Step 3]

Next, the blocking layer 7 is patterned by photolithography, forming blocking layers covering only the channel region of the i-type semiconductor layers 4.

[Step 4]

The n-type semiconductor layer 5 is formed, covering the entire surface of the unfinished product. Further, a metal layer is formed on the n-type

semiconductor layer 5.

[Step 5]

The metal film and the n-type semiconductor layer 5 are patterned by means of photolithography, forming the source electrodes 6S, the drain electrodes 6D and the drain lines DL. At the same time, the i-type semiconductor layer 4 is patterned, forming i-type semiconductor layers which define transistor regions.

Since the channel region of the n-type semiconductor layer 5 is located on the blocking layer 7, which in turn is located above the i-type semicondcutor layer 4, the i-type semiconductor laeyr 4 is not etched or damaged when the channel region of the n-type semiconductor layer 5 is removed by etching. The i-type semiconductor layer 4 remains not only in the transistor region, but also beneath the entire drain line DL.

[Step 6]

Next, the transparent conductive film of ITO or the like is formed on the gate-insulating film 3, covering the source electrode 6S, the drain electrode 6D and the drain line DL.

[Step 7]

The transparent conductive film is patterned by photolithography, thereby forming the pixel electrodes 8a.

[Step 8]

Thereafter, the protective insulation film 9 is formed.

[Step 9]

The protective insulation film 9 is patterned by photolithography, whereby its portions located on the pixel electrodes 8a and its portions located above the terminal portions DLa of the drain lines DL, and the terminal portion GLa of the gate line GL are removed. At the same time, that portion of hte gate-insulating film 3 which is located on the terminal portion GLa of the gate line GL is removed. Thus, the terminals portions DLa and GLa are thereby exposed. As a result, The TFT panel is manufactured.

In the method of manufacturing the conventional TFT panel, as many as five resist masks must be formed in order to manufacture the TFT panel. With this method, therefore, the TFT panel is manufactured but with low efficiency and at high cost. More specifically, the five resist masks are formed, respectively before:

(1) The gate metal film is patterned;
(2) The blocking layer 7 is patterned;
(3) The metal film 16 is patterned to form the source electrodes 6S and the drain electrodes 6D, and the n-type semiconductor layer 15 and the i-type semiconductor layer 14 are patterned;
(4) The transparent conductive film is patterned;
(5) The protective conductive film 9 is patterned.

Use of five resist masks leads to the necessity of preparing and using five exposure masks. The cost of preparing these exposure masks is another factor of increasing the manufacturing cost of the TFT panel.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A to 1E are cross-sectional views explaining a method of manufacturing a thin-film transistor panel which is a first embodiment of the invention;

Fig. 2 is a plan view showing a thin-film transistor panel which is a second embodiment of the invention;

Figs. 3A to 3F are cross-sectional views, explaining a method of manufacturing the thin-film transistor panel according to the second embodiment of the invention;

Fig. 4 is a plan view of the thin-film transistor panel according to the second embodiment of the present invention;

Fig. 5 is a plan view of the thin-film transistor panel according to a third embodiment of the present invention;

Figs. 6 to 8 are cross-sectional views of the thin-film transistor panel according to the third embodiment of the invention, taken along line VI-VI, VII-VII, and VIII-VIII in Fig. 5, respectively;

Figs. 9A to 9H are cross-sectional views explaining a method of manufacturing the thin-film transistor panel according to the third embodiment of the invention;

Fig. 10 is a plan view of a conventional thin-film transistor panel; and

Figs. 11 to 13 are cross-sectional views showing the conventional thin-film transistor panel, taken along lines XI-XI, XII-XII, and XIII-XIII in Fig. 10, respectively.

A thin-film transistor formed on one of the transparent substrates of an active matrix liquid-crystal display and designed for use as the active element for a pixel electrode, and an array of thin-film transistors of this type (i.e., a TFT array), being a first embodiment of the present invention, will be described with reference to Figs. 1A to 1E and Fig. 2.

Figs. 1A to 1E are cross-sectional views, each showing the thin-film transistor element and terminal portions of drain and gate lines of a TFT panel. Fig. 2 is a plan view of the thin-film transistor element and the terminals portions of the drain and gate lines.

[Step 1]

As is shown in Fig. 1A, a gate metal film of Al, an Al alloy, Cr, Ta, or the like is formed on a transparent substrate 11 made of glass or the like. The gate metal film is patterned by photolithography, forming a gate line GL and a gate electrode 12G as is shown in Fig. 2. In Fig. 1A, GLa is the terminal portion of the gate line GL.

[Step 2]

Next, as is shown in Fig. 1A, a gate-insulating film 13 made of SiN or the like is formed on the substrate 11, covering both the gate line GL and the gate electrode 12G. An i-type semiconductor layer 14 is then formed on the gate-insulating film 13. Further, an n-type semiconductor layer 15, which is made of a-Si doped with an n-type impurity, is formed on the i-type semiconductor layer 14. Still further, a metal film 16 made of Al, an Al alloy, Cr, Ta, or the like is formed on the n-type semiconductor layer 15. The film 16 will be processed to form a source electrode and a drain electrode.

[Step 3]

Then, as is shown in Fig. 1B, the metal film 16, the n-type semiconductor layer 15, and the i-type semiconductor layer 14 are patterned by photolithography, each into two portions having substantially the same size and shapes as a drain line DL (see Fig. 2) and a transistor region. In Fig. 1B, DLa is the terminal portion of the drain line DL.

[Step 4]

As is shown in Fig. 1B, too, a transparent conductive film 18 made of ITO or the like is formed on the gate-insulating film 13, thus covering the the metal film 16, already patterned.

[Step 5]

Next, as is shown in Fig. 1C, a resist mask 23 is formed on the the transparent conductive film 18. Using the mask 23, the film 18 is patterned by means of photolithography, into three portions. These three portions have the substantially the same sizes and shapes as a source electrode 16S, a drain electrode 16D, and a drain line DL, respectively, which will be formed. Using the resist mask 23 again, the metal film 16 located on the region of the transistor element is selectively etched, forming the source electrode 16S and the drain electrode 16D.

The source electrode 16S, the drain electrode 16D, and the drain line DL, which have been formed in Steps 3 to 5, consist of two layers, the lower layer being a part of the metal film 18, and the upper layer being a part of the transparent conductive film 18. A portion of the n-type semiconductor layer 15 remains beneath the drain line DL including the terminal portion DLa thereof. Also, a portion of the i-type semiconductor layer 14 remains below the drain line DL.

In the third embodiment, the transparent conductive film 18 is patterned into portions on the source electrode 16S, the drain electrode 16D and the drain line DL, these portions being a little broader than the the electrodes 16S and 16D and the drain line DL. As a result of this, the film 18 covers the electrodes 16S and 16D entirely, but the opposing sides thereof, and covers the drain line DL entirely.

[Step 6]

As is shown in Fig. 1C, using the resist mask 23 once used in patterning the transparent conductive film 18, the n-type semiconductor layer 15 is oxidized anodically, thereby electrically isolating those two parts of the layer 15 which are located beneath the source electrode 16S and the drain electrode 16D. A thin-film transistor element 10 is thereby made.

The anodic oxidation of the n-type semiconductor layer 15 is accomplished by immersing the layer 15 in an electrolytic solution, opposing the layer 15, acting as anode, to a platinum electrode (not shown) also immersed in the electrolytic solution and functioning as cathode, and applying a voltage between the layer 15 and the platinum electrode. That portion of the layer 15, which is not covered with the resist mask 23 and which contacts the electrolytic solution, undergoes a chemical reaction and is oxidized anodically. Said portion of the n-type semiconductor layer 15 is thereby changed to an insulation layer 15a.

The depth to which the n-type semiconductor layer 15 is oxidized depends, mainly on the voltage applied between the layer 15 and the platinum electrode. Hence, the selected portion of the layer 15 is anodically oxidized entirely in its thickness direction, provided that a voltage proportional to the thickness of the layer 15 is applied between the n-type semiconductor layer 15 and the platinum electrode (not shown). This is why the two parts of the

layer 15, located beneath the electrodes 16S and 16D, are electrically isolated from each other.

An electric current can be supplied to the layer 15 in order to anodically oxidize said portion of the layer 15, through the metal film 16, the transparent conductive film 18 formed on the metal film 16 and the drain electrode 16D (i.e., a part of the metal film 16). Therefore, the n-type semiconductor layers 15 of all thin-film transistor elements which are arranged along the data line DL can be anodically oxidized uniformly.

[Step 7]

Next, the resist mask 23 is removed, and a protective insulation film 17 made of SiN or the like is formed on the substrate 11, thus covering all components formed on the substrate 11, as is shown in Fig. 1D.

[Step 8]

As is shown in Fig. 1E, the protective insulation film 17 is patterned by photolithography, such that its portion on the pixel electrode 18a, its portion on the terminal portion DLa of the drain line DL, and its portion on the terminal portion GLa of the gate line GL are removed. At the same time, that portion of the gate-insulating film 13 which is located on the terminal portion GLa of the gate line GL is removed by means of etching, thereby exposing the pixel electrode 18a, the terminal portion DLa of the drain line DL, and the terminal portion GLa of the gate line GL. Thus, a TFT panel is manufactured.

In the method of manufacturing the TFT panel, described above, that portion of the n-type semiconductor layer 15, which extends between the source electrode 16S and the drain electrode 16D, is oxidized anodically, becoming an insulative layer 15a and electrically dividing the layer 15 into two portions. In other words, no part of the n-type semiconductor layer 15 is not etched away to form two n-type semiconductor layers. Hence, no damage is done to the i-type semiconductor layer 14, without forming a blocking layer on the channel region of the i-type semiconductor layer 14. The method need not have a step of forming such a blocking layer.

In the method of manufacturing a TFT panel, described above, it suffices to form only four resist masks, whereas five resist masks must be formed in the conventional method. More specifically, the four resist masks are formed, respectively before:

(1) The gate metal film is patterned;

(2) The metal film 16, the n-type semiconductor layer 15, and the i-type semiconductor layer 14 are patterned into portions having the same shape as the drain line DL and into portions having the same shape as the transistor region;

(3) The transparent conductive film 18 is patterned, the metal film 16 is divided, and the n-type semiconductor layer 15 is partly oxidized anodically;

(4) The protective insulation film 17 is patterned.

Therefore, the TFT panel can be manufactured without damaging the i-type semiconductor layer 14 and requiring less resist masks, thus with high efficiency and at low cost.

Further, since no blocking layer needs to be formed on the channel region of the i-type semiconductor layer 14, it is possible with the method to manufacture TFT panels at a higher yield than is possible with the conventional method.

In the conventional method, the etching solution applied for patterning, by photolithography, the blocking layer formed on the i-type semiconductor layer etching the blocking layer leaks to the gate-insulating film though pinholes, if any, made in the i-type semiconductor layer, inevitably forming pinholes in the gate-insulating film. These pinholes result in the short-circuiting in the thin-film transistor or at the intersections of lines (e.g., short-circuiting between the gate electrode and the source or drain electrode, and the short-circuiting between the gate line and the drain line). Consequently, the net yield of TFT panels is low.

By contrast, in the method according of this invention, no blocking layer is formed on the i-type semiconductor layer, and no step is performed to pattern such a blocking layer. It follows that the gate-insulating film need not be etched at all, for patterning such a blocking layer. Hence, no inter-layer short-circuiting occurs, whereby TFT panels can be manufactured at a high yield.

In addition, the method of this invention is characterized in that the portion of the n-type semiconductor layer, which extends between the source and drain electrodes, is anodically oxidized, becoming an insulative layer electrically dividing the n-type layer into two conductive layers. Therefore, the i-type semiconductor layer is not damaged during the manufacture of the TFT panel, and a step of forming a blocking layer is unnecessary.

Since only four resist masks need to be formed in the method of the present invention, the TFT panel can manufactured with higher efficiency and, hence, at lower cost, than in the conventional method in which four resist masks must be formed to manufacture a TFT panel of the same type.

A method of manufacturing a TFT panel, which is a second embodiment of the invention, will now be described with reference to Figs. 3A to 3F and Fig. 4. Figs. 3A to 3F are cross-sectional views explaining this method, and Fig. 4 is a plan view of the thin-film transistor panel made by this method.

[Step 1]

As is shown in Fig. 3A, a gate line GL (Fig. 4) and a gate electrode 12G are formed on a transparent substrate 11 made of glass or the like. The gate line GL consists of a lower film 12a and an upper film 12b, and the gate electrode 12G also consists of a lower film 12a and an upper film 12b. Each lower film 12a is formed on the substrate 11 and made of ITO or the like, and each upper film 12b formed on the lower film 12a and made of Al or an Al alloy. The gate line Gl and the gate electrode 12G have been made by forming a lower film on the substrate 11 and an upper film on the lower film and then by patterning both films by means of photolithography.

[Step 2]

Next, as is seen in Fig. 3A, too, a gate-insulating film 13 made of SiN or the like is formed on the substrate 11, covering the gate line GL and the gate electrode 12G. An i-type semiconductor layer 14 made of a-Si is formed on the gate-insulating film 13. An n-type semiconductor layer 15 made of a-Si doped with an n-type impurity is formed on the i-type semiconductor layer 14. Further, a contact layer 19 made of Cr or the like and provided for a source and a drain is formed on the n-type semiconductor layer 15.

[Step 3]

As is shown in Fig. 3B, the contact layer 19, the n-type semiconductor layer 15, and the i-type semiconductor layer 14 are patterned by photolithography, thereby forming a transistor region.

[Step 4]

Then, as is shown in Fig. 3C, a transparent conductive film 18 made of ITO or the like is formed on the gate-insulating film 13, covering the patterned layers 16, 15 and 14. Further, a metal film 16 made of Al or an Al alloy is formed on the conductive film 18. The metal film 16 will be processed to form a source electrode and a drain electrode.

[Step 5]

As can be understood from Fig. 3D, the metal film 16 and the transparent conductive film 18 are patterned by photolithography, forming a pixel electrode 18a, a source electrode 16S, a drain electrode 16D, and a drain line DL (see Fig. 4). Using the resist mask 21 used in patterning the films 16 and 18, the contact layer 19 is etched partly and divided into two portions, which are located below the source electrode 16S and the drain electrode 16D, respectively. In other words, that portion of the contact layer 19, which is not covered with the metal film 16 and the transparent conductive film 18, is removed by etching, thereby forming two portions which are substantially identical in size and shape to the electrodes 16S and 16D, respectively.

The source electrode 16S and the drain electrode 16D, which have been formed in Steps 3, 4, and 5, consist of three layers each, i.e., a part of the contact layer 19, a part of the conductive film 18, and a part of the metal film 16. The drain line DL consists of two layers, a part of the conductive film 18 and a part of the metal film 16.

[Step 6]

Next, as is shown in Fig. 3D, using the resist mask 21 used in patterning the metal film 16 and the conductive film 18, that portion of the n-type semiconductor layer 15 which extends between the electrodes 16S and 16D is oxidized anodically. This portion of the layer 15, which is now insulative, electrically isolates the resulting two portions of the layer 15. As a result, a thin-film transistor element 10 is formed.

The anodic oxidation of the n-type semiconductor layer 15 is achieved by immersing the substrate 11 in an electrolytic solution, opposing the layer 15, acting as anode, to a platinum electrode (not shown) also immersed in the electrolytic solution and functioning as cathode, and applying a voltage between the layer 15 and the platinum electrode. That portion of the layer 15, which is not covered with the resist mask 21 and which contacts the electrolytic solution, undergoes a chemical reaction and is oxidized anodically. This portion of the n-type semiconductor layer 15 is thereby changed to an insulation layer 15a.

The depth or thickness to which the n-type semiconductor layer 15 is oxidized depends, mainly on the voltage applied between the layer 15 and the platinum electrode. Hence, the selected portion of the layer 15 is anodically oxidized in its entirely, provided that a voltage proportional to the thickness of the layer 15 is applied between the n-type semiconductor layer 15 and the platinum electrode (not shown). This is why the two parts of the layer 15, located beneath the electrodes 16S and 16D, are electrically isolated from each other.

An electric current can be supplied to the layer 15 in order to anodically oxidize said portion of the layer 15, through the transparent conductive film 18, the drain line DL (i.e., a part of the metal film 16) formed on the film 18, and the contact layer 19 for the drain electrode 16D. Therefore, not only the

n-type semiconductor layer 15 of the thin-film transistor 10, but also the n-type semiconductor layers of other thin-film transistors (not shown), which are arranged along the data line DL, can be anodically oxidized uniformly.

[Step 7]

Next, the resist mask 21 is removed, and a protective insulation film 17 made of SiN or the like is formed on the substrate 11, thus covering all components formed on the substrate 11, as is shown in Fig. 3E.

[Step 8]

As is shown in Fig. 3E, too, the protective insulation film 17 is patterned by photolithography, such that its portion on the pixel electrode 18a, its portion on the terminal portion DLa of the drain line DL, and its portion on the terminal portion GLa of the gate line GL were removed. At the same time, that portion of the gate-insulating film 13 which is located on the terminal portion GLa of the gate line GL is removed by means of etching, thereby exposing the pixel electrode 18a, the terminal portion DLa of the drain line DL, and the terminal portion GLa of the gate line GL.

[Step 9]

Then, as can be understood from Fig. 3F, using the resist mask (not shown) once used in patterning the insulation films 17 and 13, that portion of the metal film 16 which is located on the pixel electrode 18a is removed by etching. Thereafter, the resist mask is removed, whereby a TFT panel is manufactured.

In the method according to the aforementioned embodiment of the invention, the upper film (i.e., a part of the film 16) of the terminal portion DLa and the upper film 12b (made of Al or an Al alloy) of the terminal portion GLa, both already exposed by patterning the insulation films 17 and 13, are etched when that portion of the metal film 16 which is formed on the pixel electrode 18a is etched. Nonetheless, the lower film 18 of the terminal portion DLa and the lower film 12a of the terminal portion GLa, both made of ITO or the like, are hardly etched since they are much harder to etch than the upper films of the terminal portions DLa and GLa. The lower films 18 and 12a therefore remain intact, and function as the terminal portions DLa and GLa, respectively.

In the this embodiment, the portion of the n-type semiconductor layer 15, which extends between the source and drain electrodes 16S and 16D, is anodically oxidized, becoming an insulative layer. This insulative layer electrically divides the n-type layer 15 into two conductive layers. Since no part of the n-type semiconductor layer 15 is not removed by etching as in the prior-art method, the i-type semiconductor layer 14 is not damaged during the manufacture of the TFT panel even if a blocking layer is not formed on the channel region of the layer 14. Hence, a step of forming a blocking layer is not necessary in this method, either.

Further, only four resist films need to be formed in the method according to the fourth embodiment of the invention, whereas five resist masks must be formed in the conventional method. More specifically, the four resist masks are formed, respectively before:

(1) The gate metal film 12 is patterned to form the upper and lower layers 12a and 12b;

(2) The contact layer 19, the n-type semiconductor layer 15, and the i-type semiconductor layer 14 are patterned to form the transistor region;

(3) The metal film 16 and the transparent conductive film 19 are patterned, the contact layer 19 is etched partly and divided into two portions, and the selected portion of the n-type semiconductor layer 15 is oxidized anodically;

(4) The protective insulation film 17 is patterned, that portion of the gate-insulating film 13 which is located on the terminal portion GLa of the gate line GL is removed, and that portion of the metal film 16 which is located on the pixel electrode 18a.

Therefore, the TFT panel can be manufactured by this method with higher efficiency and, thus, at lower cost, than is possible with the conventional method. Further, since no blocking layer needs to be formed on the channel region of the i-type semiconductor layer 14, TFT panels can be manufactured by the method at a higher yield than is possible with the prior-art method.

As has been described, the gate line GL and the gate electrode 12G are of two-layered structure in this embodiment, each comprised of a lower film 12a made of ITO or the like and an upper film 12b made of Al or an Al alloy. Instead, the lower film 12a may be made of Al or an Al alloy, and the upper film 12b may be made of ITO or the like, so that the terminal portion GLa of the gate line GL can remain in the form of a two-layered film.

Moreover, the gate line GL and the gate electrode 12G can be formed of only one metal film each. In the case where the line GL and the electrode 12G consist of a single metal film each, the terminal portion GLa of the gate line GL will not be etched away when the metal film 16 is partly removed to form the electrodes 16S and 16D, provided that said metal film is harder to etch than the metal film 16 or is anodically all over its sur-

face.

A method of manufacturing a TFT panel, which is a third embodiment of the invention, will now be described with reference to Figs. 5 to 8 and Figs. 9A to 9H.

The TFT panel manufactured by this method will be described first, with reference to Figs. 5 to 8. Fig. 5 is a plan view of the panel, and Figs. 6 to 8 are enlarged, cross-sectional views of the panel, taken along line XI-XI, line VII-VII and line VIII-VIII in Fig. 5, respectively.

This TFT panel comprises a transparent substrate 11 made of glass or the like, a pixel electrode 18a formed on the substrate 11, and a thin-film transistor (TFT) element 10 formed on the substrate 11 and functioning as an active element for the electrode 18a.

As is clearly seen from Figs. 5 and 6, the thin-film transistor element 10 comprises a gate electrode 12G formed on the substrate 11, a gate-insulating film 13 covering the gate electrode 12G, an i-type semiconductor layer 14 formed on a portion of the gate-insulating film 13, an n-type semiconductor layer 15 formed on the i-type semiconductor layer 14, a contact layer 19 formed on the n-type semiconductor layer 15, a source electrode 16S formed on the contact layer 19, and a drain electrode 16D formed on the contact layer 19.

The i-type semiconductor layer 14 is made of a-Si, the n-type semiconductor layer 15 is made of a-Si doped with an n-type impurity, and the contact layer 19 is formed of metal such as Cr.

The gate electrode 12G is integral with a gate line GL formed on the substrate 11. The gate-insulating film 13 covers both the gate electrode 12G and the gate line GL, and is formed on almost the entire surface of the substrate 11. The film 13 is made of SiN or the like. Formed on the gate-insulating film 13 is a data line DL which is connected to the drain electrode 16D. The gate electrode 12G and the gate line GL are formed of a gate metal film 12 which is made of aluminum or an aluminum alloy. The source electrode 16S, the drain electrode 16D, and the data line DL are formed of a drain metal film 16 which is made of aluminum or an aluminum alloy.

The pixel electrode 18a is formed on the gate-insulating film (i.e., a transparent film) 13. The electrode 18a is formed of a transparent conductive film 18 made of ITO or the like. It has an end portion formed interposed between the source contact layer 19 and source electrode 16S of the thin-film transistor element 10 and, hence, connected to the the source electrode 16S. That end portion of the pixel electrode 18a has an area smaller than that of the source electrode 16S. The source electrode 16S has a portion which does not contact the end portion of the pixel electrode 18a and which directly contacts the n-type semiconductor layer 15.

A conductive layer 18b made of the same transparent material (i.e., ITO or the like) as the pixel electrode 18a is interposed between the drain electrode 16D of the thin-film transistor element 10 and the contact layer 19 located below the drain electrode 16D. Those portions of the contact layer 19, which are located below the source and drain electrodes 16S and 16D of the transistor element 10, respectively, are identical in shape to the terminal portion of the electrode 18a and the conductive layer 18b, respectively. The conductive layer 18b and that portion of the contact layer 19, located below the drain electrode 16D, have an area each, which is smaller than that of the drain electrode 16D, and is covered with the drain electrode 16D. That portion of the drain electrode 16D, which does not cover the conductive layer 18b, contacts the n-type semiconductor layer 15 directly.

The n-type semiconductor layer 15 of the thin-film transistor element 10 is formed on the entire surface of the i-type semiconductor layer 14. That portion of the layer 15, which extends between the source electrode 16S and the drain electrode 16D, has been anodically oxidized in its entirety and, hence, is an insulative layer 15a.

The TFT panel of this embodiment has a protective insulation film 17 which is a top layer, is transparent and made of SiN or the like. As is shown in Figs. 5 and 7, the film 17 has an opening 17b. Though this opening 17b, the terminal portion DLa of the data line DL is exposed.

As is shown in Figs. 5 and 8, the terminal portion GLa of the gate line GL consists of two layers. The lower layer is a part of the gate metal film 12, and the upper film is a part of the metal film 16. The metal film 16 is laid on the lower film (i.e., a part of the gate metal film 12), filling up the opening 13a made in the gate-insulating film 13. The terminal portion GLa is exposed through the opening 17b made in the protective insulation film 17.

The TFT panel, which is the fifth embodiment of the invention, is characterized in that the portion of the n-type semiconductor layer 15, which extends between the source electrode 16S and the drain electrode 16D, is anodically oxidized, forming the insulative layer 15a which divides the layer 15 into two parts electrically isolated from each other and provided for the source and drain of the thin-film transistor 10, respectively. Therefore, this TFT panel have the same advantages as the TFT panels according to the first to fourth embodiments.

As has been indicated above, the pixel electrode 18a is interposed between the source electrode 16S and that portion of the contact layer 19

located below the source electrode 16S, and the conductive layer 18b is interposed between the drain electrode 16D of the thin-film transistor 10 and the contact layer 19 located below the drain electrode 16D. Both the electrode 18a and the conductive layer 18b are made of the same transparent material. Further, those portions of the contact layer 19, which are located below the source and drain electrodes 16S and 16D of the transistor 10, respectively, are identical in shape to the terminal portion of the electrode 18a and the conductive layer 18b, respectively. Therefore, the pixel electrode 18a and the contact layer 19 can be patterned in one and the same step.

It will now be explained how the TFT panel according to the third embodiment of the invention is manufactured, with reference to Figs. 9A to 9H which are cross-sectional views of the TFT panel.

[Step 1]

First, as is shown in Fig. 9A, the gate electrode 12G and the gate line GL (see Fig. 5) are formed on the substrate 11 made of glass or the like. The electrode 12G and the gate line GL are formed by depositing the gate metal film 12 on the substrate 11 and patterning the film 12 by means of photolithography. The metal film 12 shown at the upper-right corner of Fig. 9A is a part of the metal film 12 which is the lower film of the terminal portion GLa of the gate line GL.

[Step 2]

As is shown in Fig. 9A, too, the gate-insulating film 13 is formed on the substrate 11, covering the gate electrode 12G and the gate line GL. The i-type semiconductor layer 14 is formed on the gate insulating film 13. The n-type semiconductor layer 15 is formed on the i-type semiconductor layer 14. The contact layer 19 is formed on the n-type semiconductor layer.

[Step 3]

Next, as is shown in Fig. 9B, the contact layer 19, the n-type semiconductor layer 15, and the i-type semiconductor layer 14 are patterned by photolithography, whereby these layers 19, 15, and 14 come to have the shape and size identical to a transistor region to be formed.

[Step 4]

As is shown in Fig. 9C, the transparent conductive film 18 made of ITO or the like is formed on the substrate 11 an the gate-insulating film 13, covering the layers 14, 15, and 19 which have been patterned.

[Step 5]

As is shown in Fig. 9D, the transparent conductive film 18 is patterned by photolithography, thereby forming the pixel electrode 18a having a terminal portion located at the position where the source electrode 16S will be formed, and also forming the conductive layer 18b located at the position where the drain electrode 16D will be formed. Further, the contact layer 19 is patterned, into two contact layers which have the same shape and size as the pixel electrode 18a and the conductive layer 18b, respectively. The terminal portion of the pixel electrode 18a and the contact layer located in the source region have an area smaller than the source-electrode region. The conductive layer 18b and the contact layer located in the drain region are located fully within the drain-electrode region and have an area smaller than the drain-electrode region.

[Step 6]

As can be seen from Fig. 9D, too, an opening 13a is made in the gate-insulating film 13 by means of photolithography, thereby exposing the terminal portion GLa of the gate line GL (i.e., a part of the gate metal film 12).

[Step 7]

Next, as is shown in Fig. 9E, the metal film 16, which will be patterned to form the source electrode 16S and the drain electrode 16D, is formed on the gate-insulating film 13, covering the patterned transparent conductive film 18 and the like, and also filling the opening 13a made in the gate-insulating film 13.

[Step 8]

As is shown in Fig. 9F, the metal film 16 is patterned by photolithography, forming the source electrode 16S, the drain electrode 16D, the data line DL (see Fig. 15), and the upper film of the terminal portion GLa of the gate line GL. Both the source electrode 16S and the drain electrode 16D are large enough to cover the terminal portion of the pixel electrode 18a and the conductive layer 18b, respectively. In Fig. 17F, the terminal portion DLa of the data line DL is formed of the metal film 16 only.

[Step 9]

Then, as is shown in Fig. 9F, using the resist mask 23 which has been used in patterning the metal film 16, that portion of the n-type semiconductor layer 15, which extends between the source electrode 16S and the drain electrode 16S, is anodically oxidized in its entirety, forming the insulative layer 15a. This layer 15a divides the layer 15 into two parts electrically isolated from each other, whereby the thin-film transistor element 10 is made. The anodic oxidation of said portion of the layer 15 is performed in the same way as in any embodiments described above.

An electric current can be supplied to the layer 15 in order to achieve the anodic oxidation, through the data line DL and the drain electrode 16D. Therefore, the n-type semiconductor layers of all thin-film transistors (not shown) that are arranged along the data line DL, can be anodically oxidized uniformly. Since a resist mask 22 does not cover neither the sides of the drain electrode 16D nor the sides of the data line DL, the sides of both the electrode 16D and those of the data line DL are oxidized anodically. (The resultant oxide layers are not shown.) Nonetheless, the center portion of the electrode 16D or the center portion of the data line DL is not oxidized at all.

If the conductive layer 18b located beneath the drain electrode fourth 16D extends outwards from the drain electrode 16D and, thus, had an exposed portion, an electric current would flow between this exposed portion of the layer 18b and the platinum electrode during the anodic oxidation. (The current would continuously flow between the exposed portion of the layer 18b and the platinum electrode since the layer 18b is made of an oxide, i.e., ITO or the like.) Consequently, virtually no current would flow to the n-type semiconductor layer 15 and could not be anodically oxidized. In this embodiment, since the drain electrode 16D is large, covering up the conductive layer 18b, an electric current flows between the n-type semiconductor layer 15 and the platinum electrode, whereby that portion of the layer 15 which extends between the electrodes 16S and 16D is oxidized anodically.

[Step 10]

Then, the resist mask 22 is removed, and the protective insulation film 17 is formed as is shown in Fig. 9G.

[Step 11]

As is shown in Fig. 9H, the protective film 17 is patterned by photolithography, forming openings 17a and 17b in the film 17, thereby exposing the terminal portion DLa of the data line DL an the terminal portion GLa of the gate line GL, respectively. The TFT panel is thereby manufactured.

In the method according to the fifth embodiment of the invention, the contact layer 19 is patterned into two parts identical in shape and size to the terminal portion of the pixel electrode 18a and the conductive layer 18b, respectively, in order to pattern the transparent conductive film 18 thereby to form the pixel electrode 18a and the conductive layer 18b on those portions of the metal film 16 which will be the source electrode 16S and the drain electrode 16D, respectively. Also, the n-type semiconductor layer 15 is anodically oxidized by the use of the resist mask 22 once used in patterning the metal film 16, whereby that portion of the layer 15 between the electrodes 16S and 16D becomes the insulation layer 15a. Hence, it suffices to form less resist masks than is required in the conventional method of manufacturing TFT panels of the same type. More specifically, six resist masks are formed, respectively before:

(1) The gate metal film 12 is patterned;

(2) The contact layer 19, the n-type semiconductor layer 15, and the i-type semiconductor layer 14 are patterned to form the transistor region;

(3) The transparent conductive film 18 and the contact layer 19 beneath the film 18 are patterned;

(4) The opening 13a is formed in the gate-insulating film 13;

(5) The metal film 16 is patterned, and the n-type semiconductor layer 15 is anodically oxidized partly;

(6) The openings 17b and 17c are formed in the protective insulation film 17.

Therefore, the TFT panel can be manufactured by this method with higher efficiency and, thus, at lower cost, than is possible with the conventional method.

As has been described, the terminal portion GLa of the gate line GL is of two-layered structure comprised of a lower film formed of a part of the gate metal film 12 and an upper film formed of a part of the metal film 16. Instead, the terminal portion GLa may be comprised of a part of the gate metal film 12 only. If the portion GLa is made so, the opening 13a can be formed at the same time the openings 17b and 17a are formed in the protective insulation film 17. In this case, Step 6 need not be carried out, whereby the number of resist masks required is reduced by one.

In the third embodiment of the invention, that portion of the n-type semiconductor layer 15, which extends between the source electrode 16S and the drain electrode 16D, is oxidized in an electrolytic solution bath. Instead, this portion of the layer 15

can be oxidized by plasma oxidation which is performed in a gas atmosphere.

Claims

1. A thin-film transistor panel comprising an insulative substrate (11), a plurality of thin-film transistor elements (10) arranged at predetermined intervals on said substrate, and means (DL, GL) electrically connecting said thin-film transistor elements, characterized in that each of said thin-film transistor elements comprises:

   a gate electrode (12G);

   a gate-insulating film (13);

   an i-type semiconductor layer (14) to face the gate electrode through the gate insulating film therebetween;

   an n-type semiconductor layer (15);

   a source and drain electrodes (16S, 16D) electrically connected the portions of the i-type semiconductor layer through the n-type semiconductor layer; and

   an anodically oxidized film (15a) located between the source and drain electrodes to electrically isolate, said source and drain electrodes.

2. The thin-film transistor panel according to claim 1, characterized by further comprising a contact layer (19) located between said source electrode and said drain electrode and electrically connecting said source electrode and said drain electrode, and transparent conductive films (18) which are formed on said source electrode and said drain electrode, respectively, and which are to be processed to form pixel electrodes.

3. The thin-film transistor panel according to claim 1, characterized by further comprising a pair of contact layers (19) formed on said n-type semiconductor layer and spaced apart from each other, and transparent conductive films (18) which are to be processed to form pixel electrodes and which are interposed between one of said contact layer and said source electrode and between the other of said contact layers and said drain electrode, respectively, and electrically connecting said contact layers to said source electrode and said drain electrode, respectively.

4. The thin-film transistor panel according to claim 3, characterized in that said drain electrode, contact layer and transparent conductive film which are formed under the drain electrode have substantially same shapes.

5. A method of manufacturing a thin-film transistor panel, characterized by comprising the steps:

   a first step of forming on an insulative substrate (11), having a gate electrode (12G) formed thereon, a gate-insutating film (13), an i-type semiconductor layer (14), and an n-type semiconductor layer (15) in this order;

   a second step of forming an electrode-forming film (16) on said n-type semiconductor layer;

   a third step of patterning said electrode-forming film, thus forming a source electrode (16S) and a drain electrode (16D) which are spaced apart and located at opposing sides of a channel region; and

   a fourth step of anodically oxidizing that portion of said n-type semiconductor layer which is located in said channel region, thereby forming an insulative layer electrically isolating those portions of said n-type semiconductor layer which are located beneath said source electrode and said drain electrode, respectively.

6. The method according to claim 5, characterized in that said third step includes a first process of forming a transparent conductive film to cover at least said source and drain electrodes forming film, and a second process of patterning said transparent conductive film to separate at the channel region.

7. The method according to claim 5, characterized in that said second step includes a process of forming a transparent conductive film and the electrode forming film in this order, and said third step involves patterning said transparent conductive film and said electrode-forming film, thereby forming a conductive layer substantially identical in shape and size to a pixel electrode, and then removing the electrode-forming film which is located on the transparent conductive film and a part of said conductive layer.

8. The method according to claim 5, characterized in that said first step includes a first process of forming a contact metal layer (19) on said n-type semiconductor layer, a second process of patterning said i-type semiconductor layer and said n-type semiconductor layer, thereby forming a element region, a third process of forming a transparent conductive film (18) on said contact metal layer, and a fourth step of removing said contact metal layer and said transparent conductive film, except for those portions which are located on those por-

tions of said electrode-forming film which are to be processed to form a pixel electrode, said source electrode and said drain electrode.

9. The method according to claim 5, characterized in that said first step includes a process of forming a contact metal layer (19) on said n-type semiconductor layer, said second step involves forming said electrode-forming film on said contact metal layer, said third step involves patterning said contact metal layer, thus forming two contact metal layers spaced apart and located at opposing sides of a channel region, and which further comprises a fifth step of covering said substrate with a protective film (17) having an opening (17a) exposing said source electrode, and a sixth step of forming a pixel electrode (18a) on said protective film, extending through the opening of the protective film, and electrically connected to said source electrode.

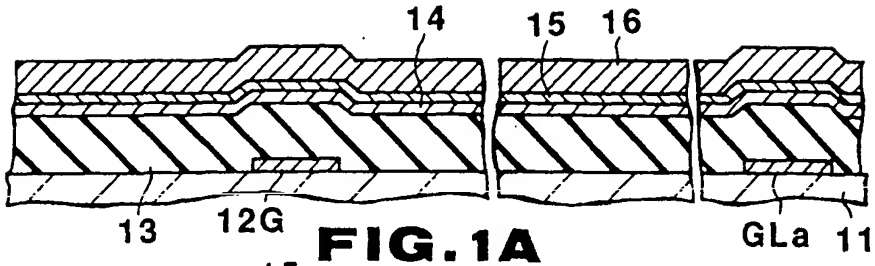


FIG.1A

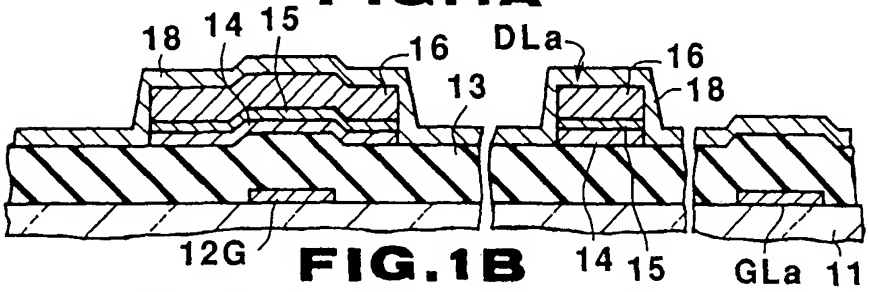


FIG.1B

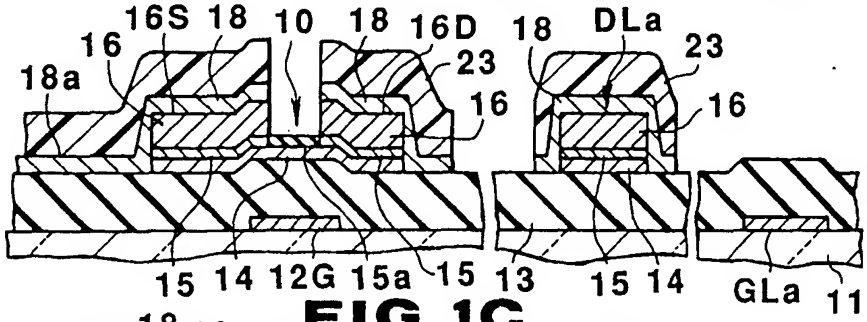


FIG.1C

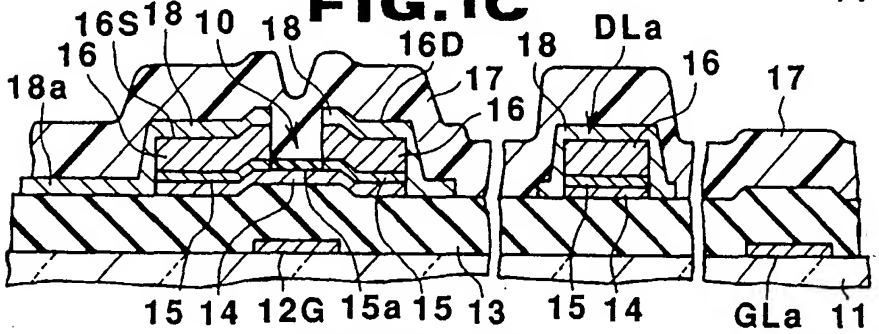


FIG.1D

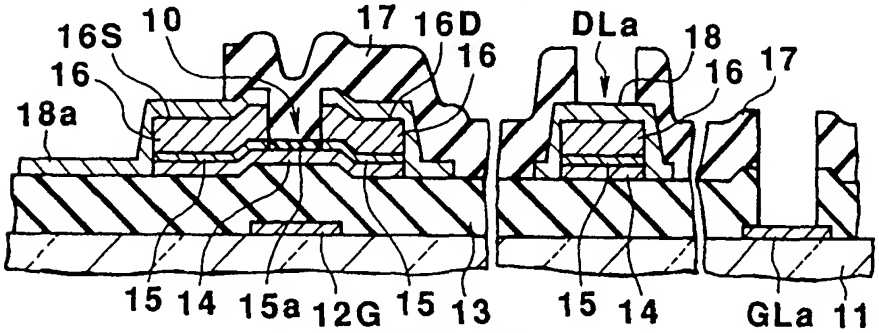


FIG.1E

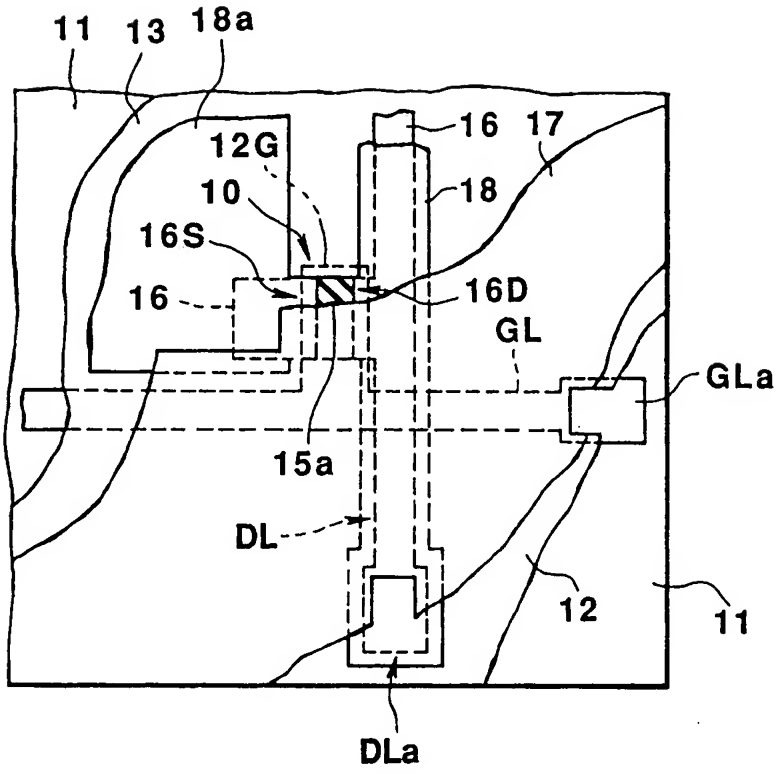


FIG.2

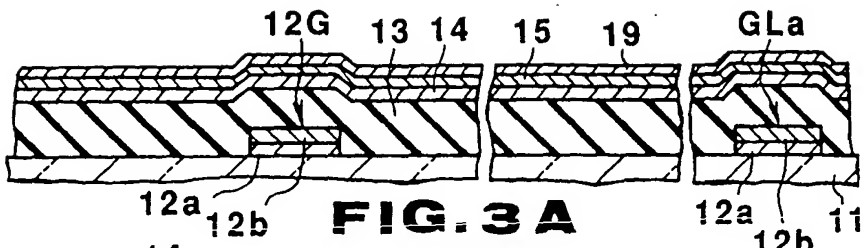


FIG. 3A

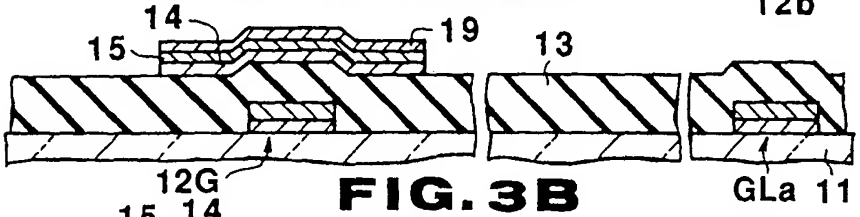


FIG. 3B

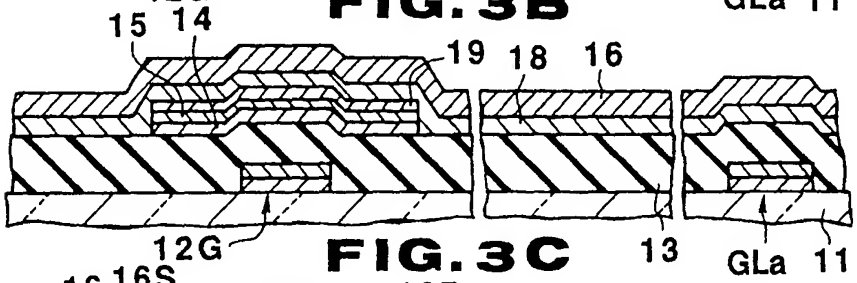


FIG. 3C

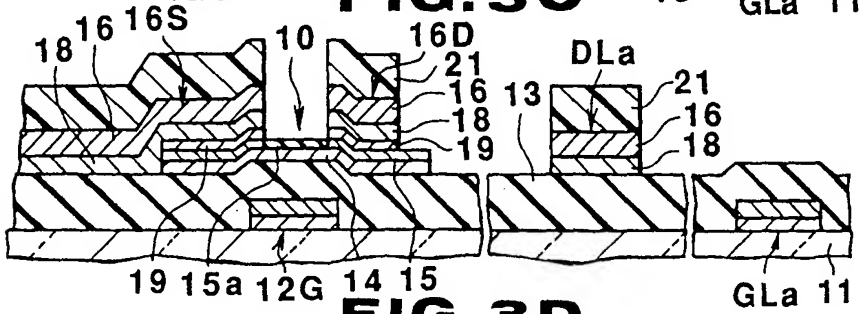


FIG. 3D

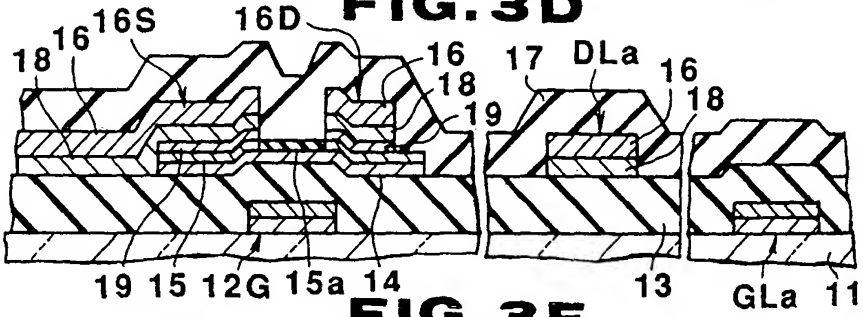


FIG. 3E

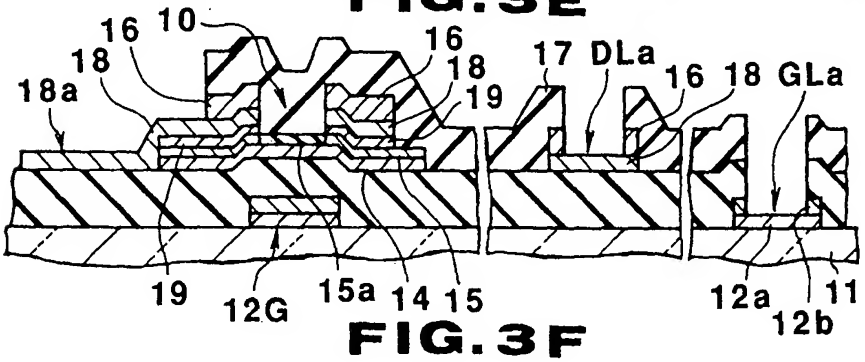


FIG. 3F

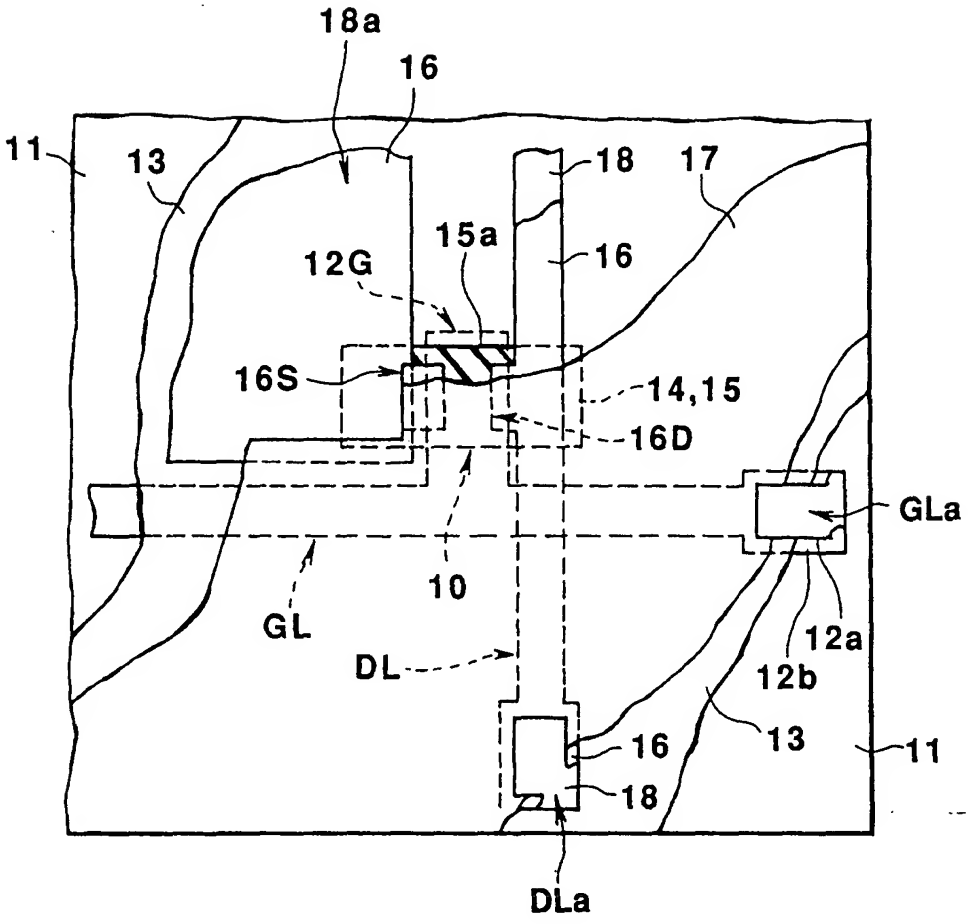
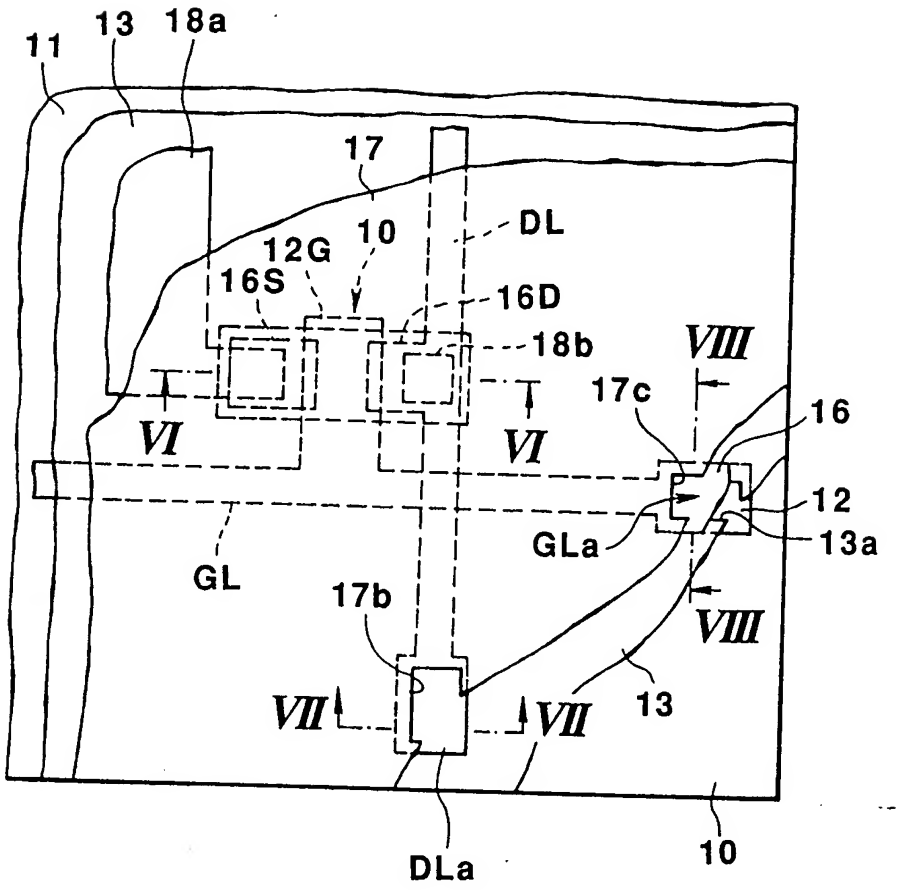

18a
16
11
13
18
17
15a
12G
16
16S
14,15
16D
GLa
10
GL
12a
12b
DL
13
16
11
18
DLa

FIG. 4


11
13
18a
17
10
12G
16S
DL
16D
18b
VIII
17c
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VI
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17b
VIII
VII
VII
13
DLa
10

FIG. 5

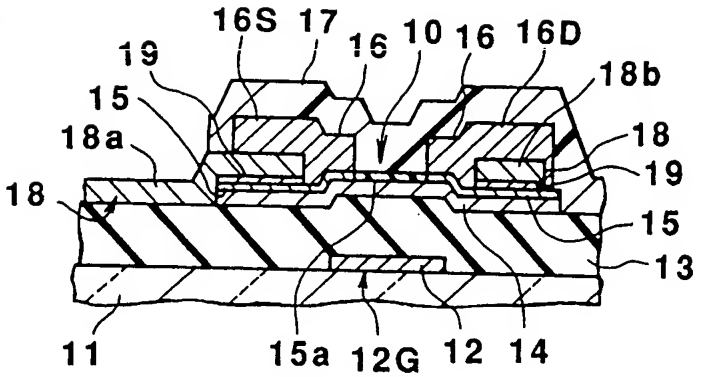

FIG.6

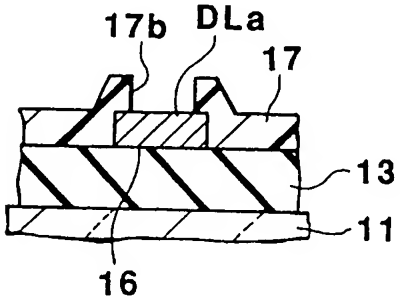

FIG.7

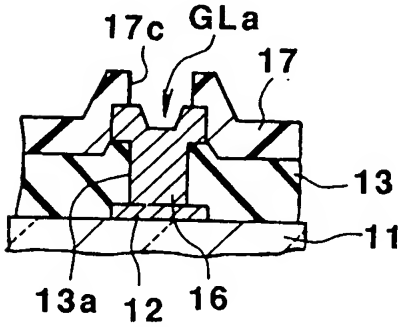

FIG.8

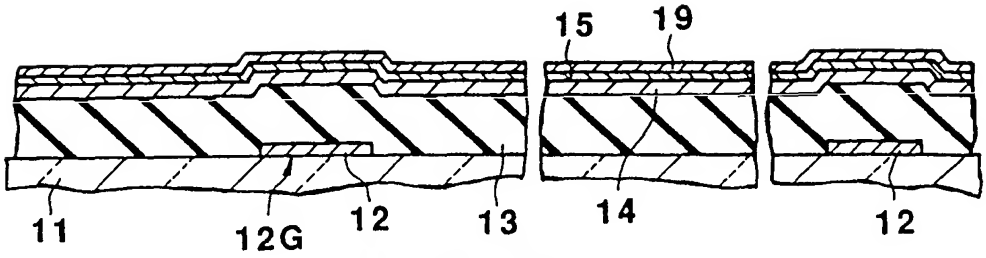

FIG. 9A

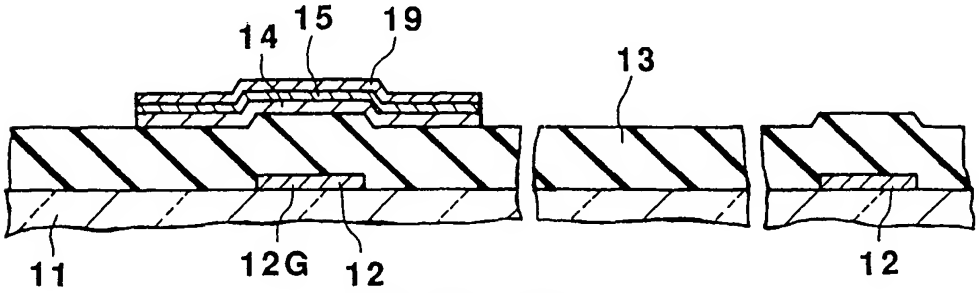

FIG. 9B

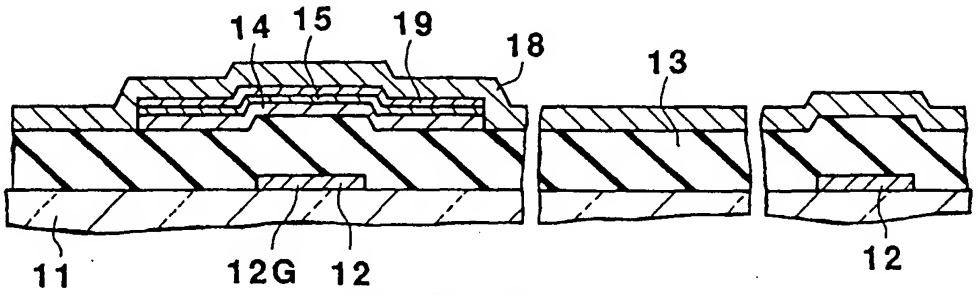

FIG. 9C

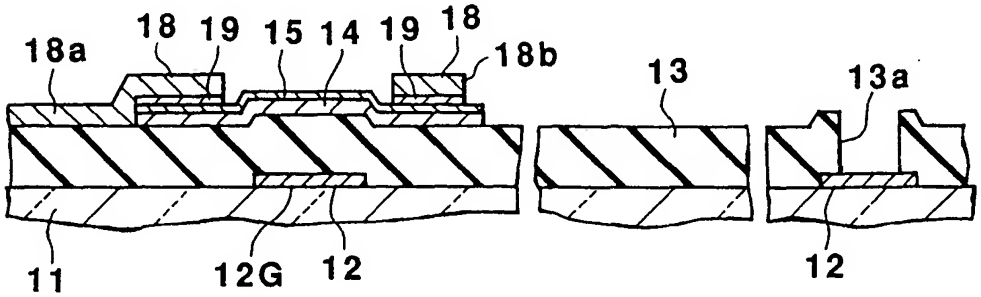

FIG. 9D

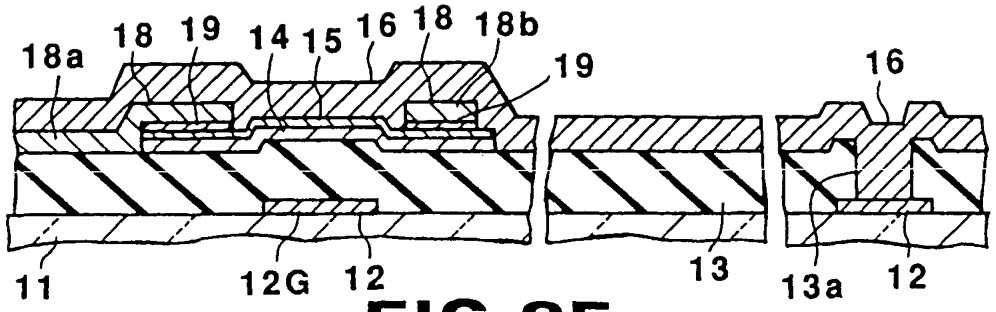

FIG. 9E

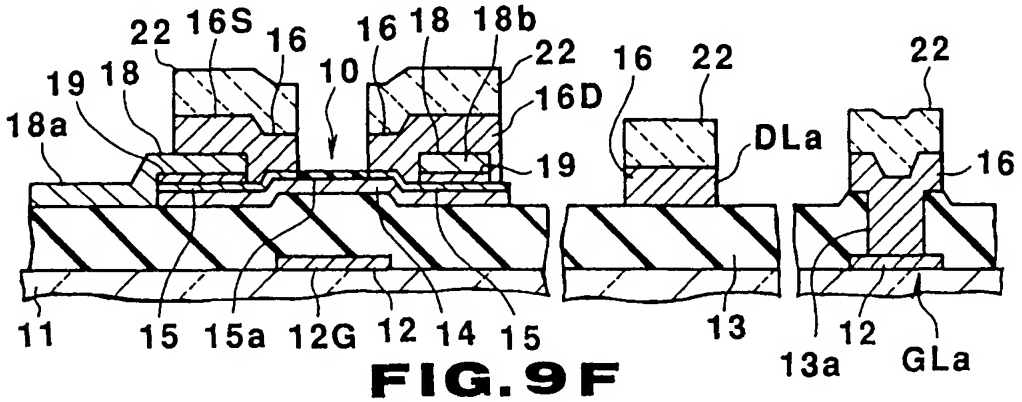

FIG. 9F

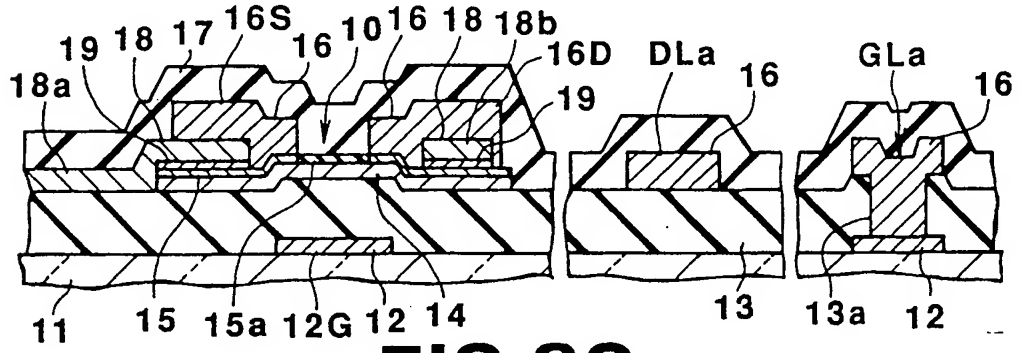

FIG. 9G

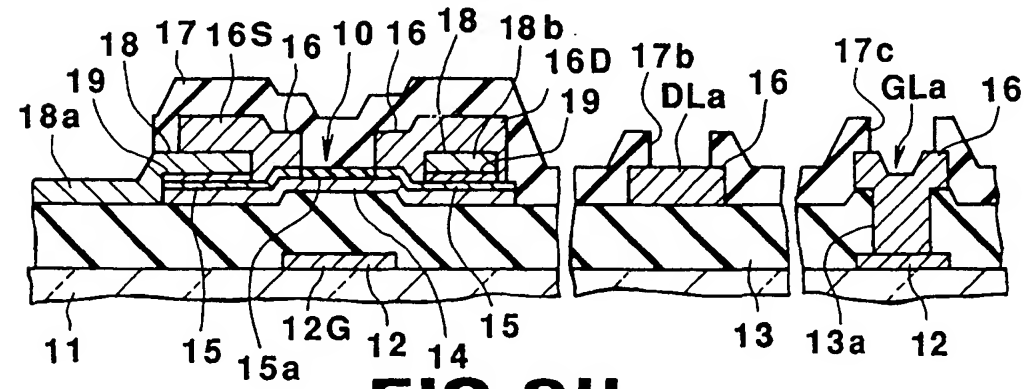

FIG. 9H

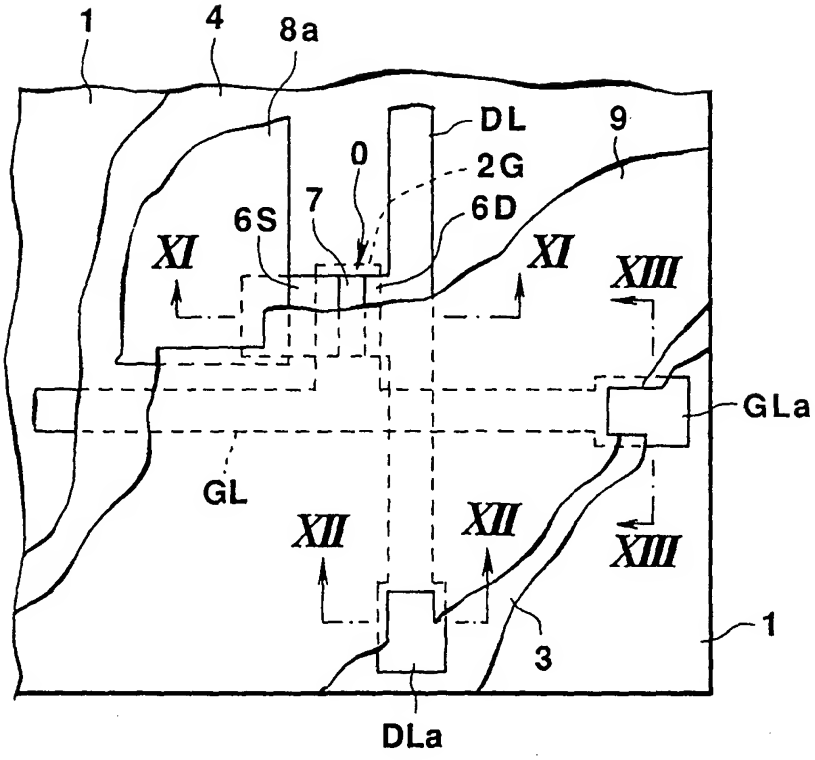

FIG.10
(PRIOR ART)

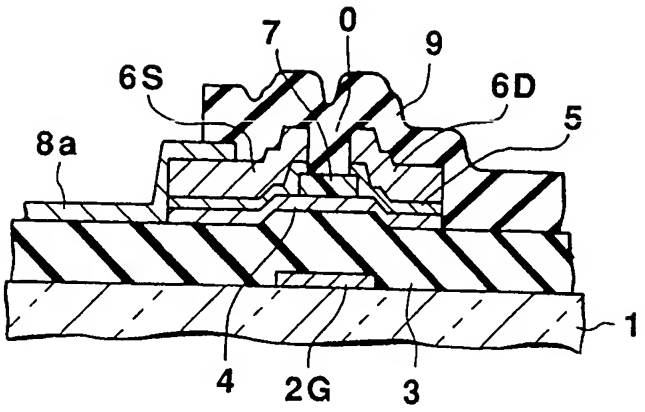

FIG.11
(PRIOR ART)

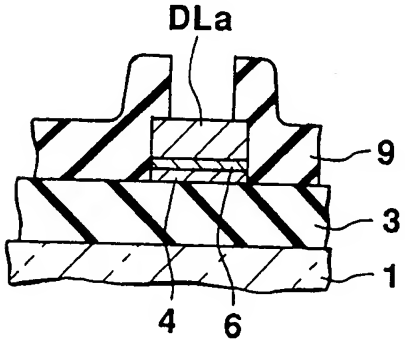

FIG.12
(PRIOR ART)

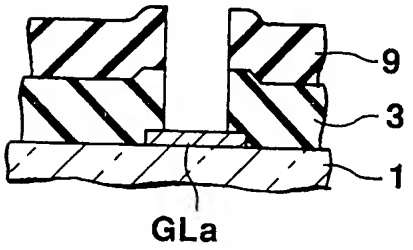

FIG.13
(PRIOR ART)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 11 5194

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	PATENT ABSTRACTS OF JAPAN vol. 10, no. 367 (E-462)(2424) 9 December 1986 & JP-A-61 164 267 (NEC) * abstract * ---	1-6,8-9	G02F1/136 H01L29/784 H01L21/336
Y	PATENT ABSTRACTS OF JAPAN vol. 10, no. 255 (E-433)2 September 1986 & JP-A-61 084 057 (FUJI XEROX) 28 April 1986 * abstract * ---	1-6,8-9	
A	EP-A-0 361 609 (PHILIPS) * claims 1-5; figure 2B * ---	1	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	14 DECEMBER 1992	MUNNIX S.

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